In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (canceled).

2. (currently amended) An automated method for designing an integrated circuit layout with a computer, comprising:

(a) selecting a plurality of cells that are intended to be used in the integrated circuit layout;

(b) determining delay values for corresponding cells in the selected plurality of cells as a function of delay to be provided by the corresponding cells and delay to be provided by loads on the corresponding cells in order to satisfy delay constraints; and

(c) performing a placement of the selected plurality of cells after determining said delay values, the placement including assigning loads for the selected plurality of cells and determining size or area of the selected plurality of cells in response to [[the]] said assigned loads and said delay values.

3-4. (canceled).

5. (previously presented) The automated method of claim 2 further comprising:

determining the size or area of the cells that will approximately maintain said delay values determined prior to said placement.

6. (canceled).

7. (previously presented) The automated method of claim 2 further comprising:

routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells.

8. (previously presented) The automated method of claim 2 wherein said delay values are determined using gain.

9. (previously presented) The automated method of claim 2 wherein said delay values are determined using logical effort.

10. (previously presented) The automated method of claim 2 wherein said delay values are determined by finding a preferred gain of the cells.

11. (previously presented) The automated method of claim 10 wherein the preferred gain of the cells is determined using a continuous buffering assumption.

12. (previously presented) The automated method of claim 2 wherein said delay values are determined during library analysis.

13. (previously presented) The automated method of claim 2 wherein said delay values are determined using a typical load of the cells.

14. (previously presented) The automated method of claim 13 wherein the typical load is determined based on gain considerations.

15. (previously presented) The automated method of claim 2 wherein the size or area of the cells is variable and not fixed at the time the cells are selected.

16. (previously presented) An automated method for designing an integrated circuit layout with a computer of a circuit specified by a netlist, comprising:

(a) providing a library of cells;

(b) determining initial delay values for a plurality of cells from said library of cells to be used in the integrated circuit layout of the circuit before determining an initial size or area of the cells, and using a timing driven covering method to map said plurality of cells to the circuit; and

(c) performing an initial placement of the cells, including assigning net lengths to nets on the cells, and determining the initial size or area of the cells in response to the initial placement.

17. (previously presented) The automated method of claim 16, including

inserting buffers based on an estimation of area savings in the circuit prior to determining said initial size or area of the cells.

18. (previously presented) The automated method of claim 16, including

compressing or stretching delay values associated with cells prior to determining said initial delay values for the cells.

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